Amendments to the Specification:

Please make the following changes to the specification –

Page	Line(s)	Description of Change
13	13	Detailed Description of ~~the Best Mode for Carrying Out the Invention~~ Figures 4-13
21	26	Although, in Fig. [[12]] 11 a 3 byte shift register implementation for performing the polynomial remaindering process is shown, a hardware shift register implementation, in the form of an application specific integrated circuit, can be produced where a two byte shift register is used
22	1-22	Referring to Fig. 12, there is illustrated step wise operation of the shift register of Fig. 11 for processing a byte data stream corresponding to a single column of user data of data frame 1000. A single column of data comprises user data bytes D_0, D_1, $D_2 \ldots D_{11,645}$. For each column, prior to entering the column of data bytes the register is initialized so that all locations are set initially to value 0 in step 1200. In step 1201, a byte shift is applied to the register so that a first byte D_0 enters the first location 1100. The remaining locations 1101, 1102 remain at value 0. A function $\cdot\alpha$ is applied to the output of the first location in step 1202 and in step 1203 there is applied an exclusive OR (XOR) of that value with the value stored in first location 1100. In step 1204, the function $\cdot\alpha$ is applied to the result of the function $\cdot\alpha$ on the content C of first location 1102. The resultant value is combined by an exclusive OR function with the content B of the second location 1101 in step 1205. In step

1206, it is checked whether all bytes of the column have been processed. If all bytes have not been processed, then the shift register is clocked to enter the next byte of the column sequence D_1 into the first location 1100. The content of first location 1100, that is the function $\cdot\alpha$ on A is shifted into the second location 1101. The previous content of the second location 1101, that is $\cdot\alpha$ applied to $\cdot\alpha$ on the content of content C of third location 1102 is shifted into the third location 1102 in step 1101. Steps 1102-1205 repeat. All bytes of the column sequence up to $D_{11,645}$ are processed in this manner. The output of the device after this process is the content of the second and ~~third~~ first locations B, A of the shift register (in step 1207).

22 24-28 Referring to Fig. 13 herein, there is illustrated operation of the function $\cdot\alpha$ on a single byte $a\cdot\alpha$ To obtain the function $\cdot\alpha$ on a 1300, denoted $a\cdot\alpha$ in step ~~1401~~ 1301 the byte a is read as a plurality of 8 individual bits a_7, a_6, a_5, a_4, a_3. a_2, a_1, a_0 into a shift register. In step 1302, the shift register is shifted left, and the least significant bit of a shift register is set at 0, giving a_6, a_5, a_4, a_3. a_2, a_1, a_0. If the

23 3 most significant bit a_7 had a value 1, then the left shifted content of the shift register is XOR'ed with a second mask function equivalent to binary value 29, i.e. 0,0,0,1,1,1,0,1 in step ~~1303~~1304. The result of the operations is an output $a\cdot\alpha$ in step 1304.